FAST UNALIGNED MEMORY ACCESS SYSTEM AND METHOD

Klaus J. Oberlaender
Erik K. Norden

ABSTRACT OF THE DISCLOSURE

A microprocessor system includes an address generator, an address selector, and memory system having multiple memory towers, which can be independently addressed. The address generator simultaneously generates a first memory address and a second memory address that is 1 row greater than the first memory address. The address selector determines whether the row portion of the first memory address or the second memory address is used for each memory tower. Because each tower can be addressed independently, a single memory access can be used to access data spanning multiple rows of the memory system.